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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,169	09/30/2003	Garo J. Derderian	M122-2373	6778
21567	7590	03/04/2004	EXAMINER	
WELLS ST. JOHN P.S. 601 W. FIRST AVENUE, SUITE 1300 SPOKANE, WA 99201			BARR, MICHAEL E	
			ART UNIT	PAPER NUMBER

1762

DATE MAILED: 03/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

AS

<b>Office Action Summary</b>	<b>Application No.</b> 10/676,169	<b>Applicant(s)</b> DERDERIAN ET AL.	
	<b>Examiner</b> Michael Barr	<b>Art Unit</b> 1762	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 49-85 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 49-85 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 9/30/03.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

## DETAILED ACTION

### *Preliminary Amendment*

1. The examiner acknowledges the cancellation of Claims 1-48 and the addition of Claims 49-85. Claims 49-85 are currently pending.

### *Double Patenting*

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 49-56, 60-61, 64-73, and 79-85 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1-11, 15-23, 41-44, and 46-48 of U.S. Patent No. 6,458,416 in view of Kang et al. Claims 1-11, 15-23, 41-44, and 46-48 of U.S. Patent No. 6,458,416 teach all of the limitations of the above mentioned claims of the present application, except that they do not teach that the substrate is a semiconductor/silicon wafer or that a portion of the substrate form a capacitor or that the deposition layer be aluminum oxide. However, Claims 1-11, 15-23, 41-44, and 46-48 of U.S. Patent No. 6,458,416 are open to any substrate and deposition materials. Kang et al. teaches depositing an aluminum oxide layer

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on a silicon semiconductor wafer substrate having a capacitor region (Abstract, Col. 7, lines 32-67). It would have been obvious to one skilled in the art to use a substrate that is a semiconductor/silicon wafer, such that a portion of the substrate form a capacitor and that the deposition layer be aluminum oxide, in the process of Claims 1-11, 15-23, 41-44, and 46-48 of U.S. Patent No. 6,458,416, with the expectation of providing the desired deposition results, since it is shown by Kang et al. that such substrate and deposition materials are known and conventional in the art and thus would be expected to be appropriate and obvious to use in the process of Claims 1-11, 15-23, 41-44, and 46-48 of U.S. Patent No. 6,458,416, which are open to the use of any substrate and deposition materials.

4. Claims 57-59, and 74-78 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1-3 and 18-22 of U.S. Patent No. 6,627,260 in view of Kang et al. Claims 1-3 and 18-22 of U.S. Patent No. 6,627,260 teach all of the limitations of the above mentioned claims of the present application, except that they do not teach that the substrate is a semiconductor/silicon wafer or that a portion of the substrate form a capacitor. However, Claims 1-3 and 18-22 of U.S. Patent No. 6,627,260 are open to any substrate materials. Kang et al. is applied here for the same reasons as given above.

5. Claims 62-63 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 7-8 of U.S. Patent No. 6,627,260 in view of Sekine et al. Claims 7-8 of U.S. Patent No. 6,627,260 teach all of the limitations of the above mentioned claims of the present application, except that they do not teach that the substrate is a silicon wafer and that the substrate include a polysilicon portion and a doped silicate portion. However, Claims 7-8 of U.S. Patent No. 6,627,260 are open to any substrate materials. Sekine et

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al. teaches depositing a coating layer on a silicon semiconductor wafer substrate having a polysilicon and doped silicate glass region (Abstract). It would have been obvious to one skilled in the art to use a substrate that is a semiconductor/silicon wafer, such that a portion of the substrate has a polysilicon and doped silicate glass regions, in the process of Claims 7-8 of U.S. Patent No. 6,627,260, with the expectation of providing the desired deposition results, since it is shown by Sekine et al. that such substrate materials are known and conventional in the art and thus would be expected to be appropriate and obvious to use in the process of Claims 7-8 of U.S. Patent No. 6,627,260, which are open the use of any substrate and deposition materials.

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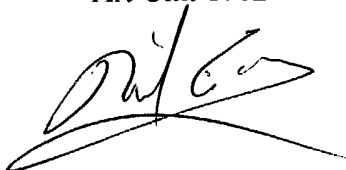
***Conclusion***

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Barr whose telephone number is 571-272-1414. The examiner can normally be reached on Monday-Thursday 6:00 am-3:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shrive Beck can be reached on 571-272-1415. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael Barr  
Primary Examiner  
Art Unit 1762

A handwritten signature in black ink, appearing to read 'Michael Barr', with a large, sweeping horizontal stroke underneath.

MB  
February 19, 2004